Book Static Timing Analysis For Nanometer Designs A

Statistical timing analysis is an area of growing importance in nanometer technology, and as the uncertainties associated with process and environmental variations increase, and this chapter has captured some of the major efforts in this area. This remains a very active field of research, and there is likely to be a great deal of new research to be found in conferences and journals after this book is published. In addition to the statistical analysis of combinational circuits, a good deal of work has been carried out in analyzing the effect of variations on clock skew. Although we will not treat this subject in this book, the reader is referred to [LNPS00, HNO1, JH01, ABZ03a] for details.

Timing Analysis for Sequential Circuits 7.1 Introduction A general sequential circuit is a network of computational nodes (gates) and memory elements (registers). The computational nodes may be conceptualized as being clustered together in an acyclic network of gates that forms a c-binarial logic circuit. A cyclic path in the direction of signal propagation 1 is permitted in the sequential circuit only if it contains at least one register. In general, it is possible to represent any sequential circuit in terms of the schematic shown in Figure 7.1, which has inputs, O outputs and M registers. The registers outputs feed into the combinational logic which, in turn, feeds the register inputs.

Thus, the combinational logic has I + M inputs and O + M outputs.

Timing, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the timing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no such book currently available that can be used by a working engineer to get acquainted with the - -t - s of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing techniques, analysis procedures and techniques. This book provides readers with an up-to-date account of the use of machine learning frameworks, methodologies, algorithms and techniques in the context of computer-aided design (CAD) for very-large-scale integrated circuits (VLSI). Coverage includes the various machine learning methods used in lithography, physical design, yield prediction, post-silicon performance analysis, reliability and failure analysis, power and thermal analysis, analog design, logic synthesis, verification, and neuromorphic design. Provides up-to-date information on machine learning in VLSI CAD for device modeling, layout verifications, yield prediction, post-silicon validation, and reliability; Discusses the use of machine learning techniques in the context of analog and digital synthesis; Demonstrates how to formulate VLSI CAD objectives as machine learning problems and provides a comprehensive treatment of their efficient solutions; Discusses the tradeoff between the cost of collecting data and prediction accuracy and provides a methodology for using prior data to reduce cost of data collection in the design, testing and validation of both analog and digital VLSI designs. From the Foreword As the semiconductor industry embraces the rising swell of cognitive systems and edge intelligence, this book could serve as a harbinger and example of the osmosis that will exist between our cognitive structures and methods, on the one hand, and the hardware architectures and technologies that will support them, on the other. As we transition from the computing era to the cognitive one, it behooves us to remember the success story of VLSI CAD and to earnestly seek the help of the invisible hand so that our future cognitive systems are used to design more powerful cognitive systems. This book is very much aligned with this ongoing transition from computing to cognition, and it is with deep pleasure that I recommend it to all those who are actively engaged in this exciting transformation. Dr. Ruchir Puri, IBM Fellow, IBM Watson CTO & Chief Architect, IBM T. J. Watson Research Center What other areas of the organization might benefit from the Static timing analysis team's improvements, knowledge, and learning? What may be the consequences for the performance of an organization if all stakeholders are not consulted regarding Static timing analysis? Who will provide the final approval of Static timing analysis deliverables? When a Static timing analysis manager recognizes a problem, what options are available? What role does communication play in the success or failure of a Static timing analysis project? Defining, designing, creating, and implementing a process to solve a challenge or meet an objective is the most valuable role... In EVERY group, company, organization and department. Unless you are talking a one-time, single-use project, there should be a process. Whether that process is managed and implemented by humans, AI, or a combination of the two, it needs to be designed by someone with a complex enough perspective to ask the right questions. Someone capable of asking the right questions and step back and say, 'What are we really trying to accomplish here? And is there a different way to look at it?' This Self-Assessment empowers people to do just that - whether their title is entrepreneur, manager, consultant, (Vice-President, CxO etc...) they are the people who rule the future. They are the person who asks the right questions to make Static timing analysis investments work better. This Static timing analysis All-Inclusive Self-Assessment enables You to be that person. All the tools you need to an in-depth Static timing analysis Self-Assessment. Featuring over 682 new and updated case-based questions, organized into seven core areas of process design, this Self-Assessment will help you identify areas in which Static timing analysis improvements can be made. In using the questions you will be better able to: - diagnose Static timing analysis projects, initiatives, organizations, businesses and processes using accepted diagnostic standards and practices - implement evidence-based best practice strategies aligned with overall goals - integrate recent advances in Static timing analysis and process design strategies into practice according to best practice guidelines Using a Self-Assessment tool known as the Static timing analysis Scorecard, you will develop a clear picture of which Static timing analysis areas need attention. Your purchase includes access details to the Static timing analysis self-assessment dashboard download which gives you your dynamically prioritized projects tool and shows your organization exactly what to do next. Your exclusive instant access details can be found in your book.

As the feature size decreases in deep sub-micron designs, coupling capacitance becomes the dominant factor in total capacitance. The resulting crosstalk noise may be responsible for signal integrity issues and significant timing variation. Traditionally, static timing analysis tools have ignored cross coupling effects between wires altogether. Newer tools simply approximate the coupling capacitance by a 2X Miller factor in order to compute the worst case delay. The latter approach not only reduces delay calculation accuracy, but can also be shown to underestimate the delay in certain scenarios. This book describes accurate but conservative methods for computing delay variation due to coupling. Furthermore, most of these methods are computationally efficient enough to be employed in a static timing analysis tool for complex integrated digital circuits. To achieve accuracy, a more accurate computation of the Miller factor is derived. To achieve both computational efficiency and accuracy, a variety of mechanisms for pruning the search space are detailed, including: - Spatial pruning - reducing aggressors to those in physical proximity, - Electrical pruning - reducing aggressors by electrical strength, - Temporal pruning - reducing aggressors using timing windows, - Functional pruning - reducing aggressors by Boolean functional analysis. Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting...
from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

Single-threaded software applications have ceased to see gains in performance on a general-purpose CPU, even with further scaling in very large scale integration (VLSI) technology. This is a significant problem for electronic design automation (EDA) applications, since the design complexity of VLSI integrated circuits (ICs) is continuously increasing. In this research monograph, we evaluate custom ICs, field-programmable gate arrays (FPGAs), and graphics processors as platforms for accelerating EDA algorithms, instead of the general-purpose single-threaded CPU. We study applications which are used in key time-consuming steps of the VLSI design flow. Further, these applications also have different degrees of inherent parallelism in them. We study both control-dominated EDA applications and control plus data parallel EDA applications. We accelerate these applications on different hardware platforms. We also present an automated approach for accelerating certain uniprocessor applications on a graphics processor. This monograph compares custom ICs, FPGAs, and graphics processing units (GPUs) as potential platforms to accelerate EDA algorithms. It also provides details of the programming model used for interfacing with the GPUs.

This book provides a comprehensive overview of characterization techniques and advanced modeling of VLSI circuits for modern and advanced process nodes for timing, power, noise and variation models. Intended audience includes research professionals, graduate students, circuit and PDK designers, characterization engineers, CAD developers, managers, mentors, and the merely curious. It is organized to serve as a compendium to a beginner, a ready reference to intermediate and source for an expert.

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

If you can spare half an hour, then this ebook guarantees job search success with VLSI interview questions. Now you can ace all your interviews as you will access to the answers to the questions, which are most likely to be asked during VLSI interviews. You can do this completely risk free, as this book comes with 100% money back guarantee. To find out more details including what type of other questions book contains, please click on the BUY link.

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.

This book provides a single-source reference to the state-of-the-art in logic synthesis. Readers will benefit from the authors’ expert perspectives on new technologies and logic synthesis, new data structures, big data and logic synthesis, and convergent logic synthesis. The authors describe techniques that will enable readers to take advantage of recent advances in big data techniques and frameworks in order to have better logic synthesis algorithms.

Static Timing Analysis for Nanometer DesignsA Practical Approach Springer Science & Business Media

This book describes a novel approach for the design of embedded systems and industrial automation systems, using a unified model-driven approach that is applicable in both domains. The authors illustrate their methodology, using the IEC 61499 standard as the main vehicle for specification, verification, static timing analysis and automated code synthesis. The well-known synchronous approach is used as the main vehicle for defining an unambiguous semantics that ensures determinism and deadlock freedom. The proposed approach also ensures very efficient implementations either on small-scale embedded devices or on industry-scale programmable automation controllers (PACs). It can be used for both centralized and distributed implementations. Significantly, the proposed approach can be used without the need for any run-time support. This approach, for the first time, blurs the gap between embedded systems and automation systems and can be applied in wide-
ranging applications in automotive, robotics, and industrial control systems. Several realistic examples are used to demonstrate for readers how the methodology can enable them to reduce the time-to-market, while improving the design quality and productivity.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® Physical Compiler® and PrimeTime®, Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

Designus Maximus Unleashed! is more than a collection of article reprints; in this book, the original (unedited) text is revisited, along with new insights and previously unpublished material, all presented in the author's distinctive personal style. The accompanying CD-ROM includes a fully-functioning virtual computer, as well as BOOL Logic Synthesis, MMLogic Multimedia Logic Design System, and Analog Magic. Clive Maxfield, a popular columnist, has collected his articles in a new order, grouped by topic, and expanded from the limits of magazine space. These articles have been published in magazines such as EDN, Electronic Design, and Electronic Design & Technology. In addition, he includes new material such as the history of computing, logic design tools, and the virtual computer. Two chapters of personal perspective begin and end the text. Clive 'Max' Maxfield received his B.Sc. in Control Engineering from Sheffield Polytechnic (now Sheffield Hallam University), England, and began his career as a mainframe CPU designer. He is currently a Member of the Technical Staff at Intergraph Computer Systems, Huntsville AL. In his spare time, Max is a contributing editor to EDN magazine and a member of the advisory board to the Computer History Association of California. In addition to numerous technical articles and papers, Max is also the author of Bebop to the Boolean Boogie and the co-author of Bebop Bytes Back (An Unconventional Guide to Computers). Based primarily on Designus Maximus series of articles from EDN magazine with new chapters and expanded text Includes a CD-ROM including the Beboputer: Virtual Computer Written by a popular columnist

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices. Readers will benefit from the hands-on approach which starts form the ground-up, explaining with basic examples what power is, how it is measured and how it impacts on the design process of application-specific integrated circuits (ASICs). The authors use both the Unified Power Format (UPF) and Common Power Format (CPF) to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent. From analyzing system power consumption, to techniques that can be employed in a low power design, to a detailed description of two alternate standards for capturing the power directives at various phases of the design, this book is filled with information that will give ASIC designers a competitive edge in low-power design.

If you can spare half an hour, then this e-book guarantees job search success with STA interview questions. Now you can ace all your interviews as you will access to the answers to the questions, which are most likely to be asked during VLSI interviews. You can do this completely risk free, as this book comes with 100% money back guarantee. To find out more details including what type of other questions book contains, please click on the BUY link.

Introduction to Sports Biomechanics has been developed to introduce you to the core topics covered in the first two years of your degree. It will give you a sound grounding in both the theoretical and practical aspects of the subject. Part One covers the anatomical and mechanical foundations of biomechanics and Part Two concentrates on the measuring techniques which sports biomechanists use to study the movements of the sports performer. In addition, the book is highly illustrated with line drawings and photographs which help to reinforce explanations and examples.

Until now, there has been a lack of a complete knowledge base to fully comprehend Low power (LP) design and power aware (PA) verification techniques and methodologies and deploy them all together in a real design verification and implementation project. This book is a first approach to establishing a comprehensive PA knowledge base. LP design, PA verification, and Unified Power Format (UPF) or IEEE-1801 power format standards are no longer special features. These technologies and methodologies are now part of industry-standard design, verification, and implementation flows (DVIF). Almost every chip design today incorporates some kind of low power technique either through power management on chip, by dividing the design into different voltage areas and controlling the voltages, through PA dynamic and PA static verification, or their combination. The entire LP design and PA verification process involves thousands of techniques, tools, and methodologies, employed from the register transfer level (RTL) of design abstraction down to the synthesis or place-and-route levels of physical design. These techniques, tools, and methodologies are evolving everyday through the progression of design-verification complexity and more intelligent ways of handling that complexity by engineers, researchers, and corporate engineering policy makers.

Arranged in a format that follows the industry-common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally, testing. Among the topics covered are Basic standard cell design, transistor-sizing, and layout styles; Linear, non-linear, and polynomial characterization; Physical design constraints and floorplanning styles; Algorithms used for placement; Clock Tree Synthesis; Parasitic extraction; Electronic Testing, and many more.

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs.
comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design. Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter System™. However, if the reader uses a different EDA tool, that tool’s commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Flooormap and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

Reviewers tell us that Case/Fair is one of the all-time bestselling principles of economics texts because they trust it to be clear, thorough and complete. This well-respected author team is joined for the 9th edition by a new co-author, Sharon Oster. Sharon's research and teaching experience brings new coverage of modern topics and an applied approach to economic theory, as demonstrated in the new Economics in Practice feature. Introduction to Economics: Concepts and Problems in Macroeconomics; The Core of Macroeconomic Theory; Further Macroeconomic Issues; The World Economy For those looking for a trusted and authoritative principles of macroeconomics text that focuses on international economics as well as the Keynesian Cross. Case/Fair/Oster believe strongly, that a text should use the Keynesian Cross carefully and systematically, to build up to the AD/AS model. One of the great benefits of this approach, is that students of economics won't mistakenly apply what they learned about supply and demand to aggregate demand & supply. (A detailed summary of this approach can be found in the preface). From ASICs to SOCs: A Practical Approach, by Farzad Nekoogar and Faranak Nekoogar, covers the techniques, principles, and everyday realities of designing ASICs and SOCs. Material includes current issues in the field, front-end and back-end designs, integration of IPs on SOC designs, and low-power design techniques and methodologies. Appropriate for practicing chip designers as well as graduate students in electrical engineering.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: 'This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

Since register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design. The book gives an understanding of the underlying principles of advanced ASIC technology. It not only focuses on circuit design process obeying VLSI rules but also on technological aspects of prototyping and fabrication. All the clocking processes, interconnects, and circuits of CMOS are explained in this book in an understandable format. The book provides contents on VLSI Physical Design Automation, Design of VLSI Devices and also its Impact on Physical Design.

Field Programmable Gate Arrays (FPGAs) are devices that provide a fast, low-cost way for embedded system designers to customize products and deliver new versions with upgraded features, because they can handle very complicated functions, and be reconfigured an infinite number of times. In addition to introducing the various architectural features available in the latest generation of FPGAs, The Design Warrior’s Guide to FPGAs also covers different design tools and flows. This book covers information ranging from schematic-driven entry, through traditional HDL/RTL-based simulation and logic synthesis, all the way up to the current state-of-the-art in pure C/C++ design capture and synthesis technology. Also discussed are specialist areas such as mixed hardware/software and DSP-based design flows, along with innovative new devices such as field programmable node arrays (FPNAs). Clive "Max" Maxfield is a bestselling author and engineer with a large following in the electronic design automation (EDA) and embedded systems industry. In this comprehensive book, he covers all the issues of interest to designers working with, or contemplating a move to, FPGAs in their product designs. While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems. First book to focus exclusively and comprehensively on FPGA use in embedded designs World-renowned best-selling author Will help engineers get familiar and succeed with this new technology by providing much-needed advice on choosing the right FPGA for any design.
Research and development of logic synthesis and verification have matured considerably over the past two decades. Many commercial products are available, and they have been critical in harnessing advances in fabrication technology to produce today's plethora of electronic components. While this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges. Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references. Two unique features of this book are technical strength and comprehensiveness. The book chapters are written by twenty-eight recognized leaders in the field and reviewed by equally qualified experts. The topics collectively span the field. Logic Synthesis and Verification fills a current gap in the existing CAD literature. Each chapter contains essential information to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools. From the foreword: “The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book. Their innovative work contributed to design automation tools that permanently changed the course of electronic design.” by Aart J. de Geus, Chairman and CEO, Synopsys, Inc.

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.

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